TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. END920030032US1

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AUG 07 2006
PATENT & TRADEMARK

In Re Application Of: **Ramindcrpal Singh, et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/665,993	September 18, 2003	Victor A. Mandala	23389	2826	6599

Invention: **A VERTICALLY-STACKED CO-PLANAR TRANSMISSION LINE STRUCTURE FOR IC DESIGN**

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Dated: **July 28, 2006**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Raminderpal Singh, et al.

Examiner: Victor A. Mandala

Serial No.: 10/665,993

Art Unit: 2826

Filed: September 18, 2003

Docket: END920030032US1 (16704)

For: A VERTICALLY-STACKED CO-PLANAR TRANSMISSION LINE STRUCTURE FOR IC DESIGN

Dated: July 28, 2006

Conf. No.: 6599

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APPEAL BRIEF

Sir

Pursuant to 35 U.S.C. § 134 and 37 C.F.R. § § 1.191 and 1.192, entry of this Appeal Brief in support of the Notice of Appeal filed May 30, 2006 in the above-identified matter is respectfully requested. This paper is submitted as a brief setting forth the authorities and arguments upon which Appellants rely in support of the appeal from the Final Rejection of Claims 1-4, 7 and 8 in the above-identified patent application on January 30, 2006.

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Dated: July 28, 2006

Steven Fischman

1. STATEMENT OF REAL PARTY OF INTEREST

The real party of interest in the above-identified patent application is International Business Machines Corporation.

2. STATEMENT OF RELATED APPEALS AND INTERFERENCES

There are no pending appeals or interferences related to this application to Appellants' knowledge.

3. STATEMENT OF THE STATUS OF THE CLAIMS

A. Claim Status

Claims 1-4 and 7-8 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application No. 2004/0222859 to Hajimiri et al. ("Hajimiri").

B. Appealed Claims

Claims 1-4 and 7-8 are appealed, a clean copy of which are attached hereto in Appendix A.

4. STATEMENT OF STATUS OF AMENDMENTS

Claim 1 was amended in a Response to the Final Rejection filed March 30, 2006. The claim amendments were considered and not entered by the Examiner for the purposes of appeal.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The invention with respect to claim 1 comprises a vertically stacked coplanar transmission line structure for an integrated circuit (IC) chip defining a closed ground return path within the transmission line structure, comprising:a micro-strip pair of first and second vertically stacked coplanar conductors, each first and second vertical stack comprising a metal layer, a next metal layer down, and an intermediate connecting via layer in between the metal layer and the next metal layer down, said intermediate connecting via layer comprising a via bar having a width dimension approximately equal to a width dimension of the first and second vertically stacked coplanar conductors and having a length dimension approximately equal to a length dimension of the first and second vertically stacked coplanar conductors. (See Fig. 1, paragraph [0017] bridging pages 3 and 4 and page 4, paragraph [0019] of the present specification).

The invention with respect to claim 2 comprises the transmission line structure as in claim 1, wherein each vertically stacked coplanar conductor comprises metal in the metal layer m(i), metal in the next metal layer down m(i-1), and metal in the intermediate connecting via layer (See page 4, paragraph [0019] of the present specification).

The invention with respect to claim 3 comprises the transmission line structure of claim 1, fabricated in upper metal layers of the IC chip. (See page 2, paragraph [0010] of the present specification)

The invention with respect to claim 4 comprises the transmission line structure of claim 1, wherein the intermediate connecting via layer comprises a single via bar which extends across an entire width of the intermediate connecting via layer. (See Fig. 1, paragraph [0017] bridging pages 3 and 4).

The invention with respect to claim 7 comprises the transmission line structure of claim 1,

wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise a differential positive and negative pair of transmission line conductors. (See Fig. 3(a), page 5, paragraph [0022] of the specification).

The invention with respect to claim 8 comprises the transmission line structure of claim 1, wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise signal and ground transmission line conductors. (See Fig. 3(b), page 5, paragraph [0023] of the specification).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review are whether claims 1-4, and 7-8 are anticipated by Hajimiri.

7. ARGUMENTS

A. The rejection of claims 1-4 and 7-8, on appeal, under 35 U.S.C. § 102(b), as being anticipated by Hajimiri et al., is improper.

1. Claim 1

In the Final Official Action issued January 30, 2006, the Examiner rejected pending claims 1-4 and 7-8 under §102(b) as being anticipated by Hajimiri, et al.

In a Response, filed March 30, 2006, Appellants amended Claim 1 and made arguments that the cited reference did not teach or suggest Appellants' invention.

In the Advisory Action issued May 4, 2006, the Examiner considered Appellants' claim amendments and arguments, but found they allegedly raised new issues requiring further search or consideration. However, the Examiner indicated that Appellants' claim amendments

would not be entered for purposes of appeal.

Appellants respectfully disagree with the Examiner's characterization and interpretation of the reference cited and discussed in the Final Office Action.

With respect to independent Claim 1, the Final Office Action states that Hajimiri teaches all of Appellants' recited elements, i.e., a microstrip pair of vertically stacked coplanar transmission line structure for an IC (integrated circuit chip).

Appellants' independent claim 1 recites a vertically stacked coplanar transmission line structure for an integrated circuit (IC) chip defining a closed ground return path within the transmission line structure, comprising: a micro-strip pair of first and second vertically stacked coplanar conductors, each first and second vertical stack comprising a metal layer, a next metal layer down, and an intermediate connecting via layer in between the metal layer and the next metal layer down, said intermediate connecting via layer comprising a via bar having a width dimension approximately equal to a width dimension of the first and second vertically stacked coplanar conductors and having a length dimension approximately equal to a length dimension of the first and second vertically stacked coplanar conductors.

Hajimiri, to the contrary, is directed to the field of distributed oscillators, particularly, oscillators that will be integrated within an IC, and is therefore not analogous to micro-strip pair IC transmission line technology as claimed in Claim 1, which is otherwise known as a waveguide (See present specification at page 2, paragraph [0006]). The fact that Hajimiri's device is incorporated in an IC is where any degree of similarity ends. The Examiner, in the final rejection, nonetheless indicates that page 3, paragraph [0028] of Hajimiri coupled with the accompanying drawings of Figures 5A-5B of Hajimiri, allegedly anticipates Claim 1 as amended.

While entitled to a broad reading of the claims, the Examiner misinterprets Hajimiri

by indicating that it is a microstrip structure. Respectfully, in transmission line theory, a micro-strip pair has a specific meaning and structure for generating electric field patterns, e.g., those associated with non-TEM (transverse electromagnetic mode) of signal propagation.

To the contrary, Hajimiri is directed to an oscillator structure comprising a four (4) port structure having two transmission lines each with an amplifier device interconnecting the two transmission lines (See Hajimiri Figure 5A, amplification device 608 interconnecting input transmission line 602 and output transmission line 604). The Examiner particularly cites Hajimiri page 3, parag. [0028] and the teachings of Figure 5A and 5B as teaching the present invention. However, Hajimiri does not provide a microstrip structure having two stacked coplanar transmission line structures of the micro-strip pair. That is, Hajimiri's structure is not a "stacked" transmission line structure as in the present invention claimed in Claim 1 but rather, is a specially configured amplifier structure (a traveling-wave amplifier structure or TWAS as shown in Figure 2 of Hajimiri) that functions as an oscillator. There is no teaching or suggestion in Hajimiri that is directed to provision of a conductive via layer in intermediate connection with the top metal layer and underlying metal layer in each vertically stacked structure of the microstrip pair as claimed in the present invention. Hajimiri rather discusses an input transmission line (conductor 602 in Figure 5A of Hajimiri) and an output transmission line (conductor 604) shown interconnected with an amplifier device (transistor 608) forming part of a distributed oscillator (element 600B of Hajimiri Figure 5B). A further transmission line (third transmission line 606) is interconnected with the second transmission line 604 by a further amplification device (transistor 610).

The Examiner in the Final Official Action rejection further likens a third transmission line (element 604) in Figure 5A as an intermediate connecting via layer in between two metal layers 606 and 602. However, this is not an interconnecting via as contemplated and taught in

the micro-strip pair of first and second vertically stacked coplanar conductors of the present invention as claimed in Claim 1. The term via has associated meaning to a skilled artisan as a passive conductor layer that interconnects two conductor (metal) layers and electrically couples the metal layers. A via layer is not a transmission line. In the present invention, the microstrip pair comprises a first vertical stack and a second vertical stack in a coplanar configuration, each vertical stack having two layers of metal and an interconnecting via metal layer therebetween comprising a via bar. In Hajimiri, the layer that the Examiner likens the claimed via bar in Claim 1 to the output transmission line 604 (Hajimiri, Figure 5A) that couples the two transmission lines (602, 606 of Hajimiri Fig. 5A) via active devices (amplifiers 608, 610). Thus, the Examiner's characterization of Hajimiri's layer 604 as a via layer is incorrect.

Moreover, in Hajimiri, the trio of conductors transmission lines 602, 604 and 606, do not form a stacked structure (the word "stack" does not appear in the Hajimiri at all) and is contrary to the typically meaning of a stack as known to skilled artisans familiar with CMOS device manufacturing technology.

Moreover, notwithstanding Hajimiri's Figure 5A which show approximately equal width and length dimensions for each transmission line (602, 604 and 606) as shown in Figure 5A, it is respectfully submitted that Hajimiri disclosure is actually silent as to the length and width dimensions of the three transmission lines. The dimensions of these transmission lines 602, 604 and 606 are presented similar in dimension for purposes of illustration and, in fact, appear to extend further out as indicated by the dashed lines at each end. Thus, it can not be relied on for certainty that Hajimiri teaches structures having equal width and length. In fact, the discussion of Hajimiri on page 3, paragraph [0031] indicates that embodiments for the distributed oscillator may take the form of straight, square, and polyhedron or other suitable shapes /configurations.

In view of the foregoing, it is respectfully submitted that Hajimiri does not teach or suggest the subject matter recited in Appellants' independent Claim 1. Specifically, Hajimiri does not teach or suggest a vertically stacked coplanar transmission line structure for an integrated circuit (IC) chip defining a closed ground return path within the transmission line structure.

2. Claims 2-3, and 7-8

Claims 2-3, and 7-8, which depend directly from independent claim 1, incorporate all of the limitations the corresponding independent claim and are therefore patentably distinct over Hajimiri for at least those reasons provided for claim 1.

Respectfully submitted,

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APPENDIX A

CLAIMS ON APPEAL: CLAIMS 1-3, 5-12, and 14-19
Application Serial No. 10/420,151

1. (Rejected) A vertically stacked coplanar transmission line structure for an integrated circuit (IC) chip defining a closed ground return path within the transmission line structure, comprising:

a micro-strip pair of first and second vertically stacked coplanar conductors, each first and second vertical stack comprising a metal layer, a next metal layer down, and an intermediate connecting via layer in between the metal layer and the next metal layer down, said intermediate connecting via layer comprising a via bar having a width dimension approximately equal to a width dimension of said first and second vertically stacked coplanar conductors and having a length dimension approximately equal to a length dimension of said first and second vertically stacked coplanar conductors.

2. (Rejected) The transmission line structure of claim 1, wherein each vertically stacked coplanar conductor comprises metal in the metal layer m(i), metal in the next metal layer down m(i-1), and metal in the intermediate connecting via layer.

3. (Rejected) The transmission line structure of claim 1, fabricated in upper metal layers of the IC chip.

4. (Rejected) The transmission line structure of claim 1, wherein the intermediate connecting via layer comprises a single via bar which extends across an entire width of the intermediate connecting via layer.

7. (Rejected) The transmission line structure of claim 1, wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise a differential positive and negative pair of transmission line conductors.

8. (Rejected) The transmission line structure of claim 1, wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise signal and ground transmission line conductors.

APPENDIX B

EVIDENCE SUBMITTED
Application Serial No. 10/665,993

There is no evidence relied upon by the Appellants in this appeal.

APPENDIX C

RELATED PROCEEDINGS
Application Serial No. 10/665,993

There are no pending appeals or interferences related to this application to Appellants' knowledge.